YCHIOT MAX5007

LONG RANGE UWB MODULE

DATASHEET

Version 1.3

YCHIOT MAX5007-UWB Module Features Overview

The MAX5007 module is an ultra-wideband transceiver module based on the DW1000 chip design of decaWave, which is self-developed by YCHIOT. The module integrates the antenna and all radio frequency circuits, power management and clock circuits. This module can be used in TWR or TDOA positioning systems to locate targets with an accuracy of less than 10cm; and the module supports data transmission rates up to 6.8Mbps.
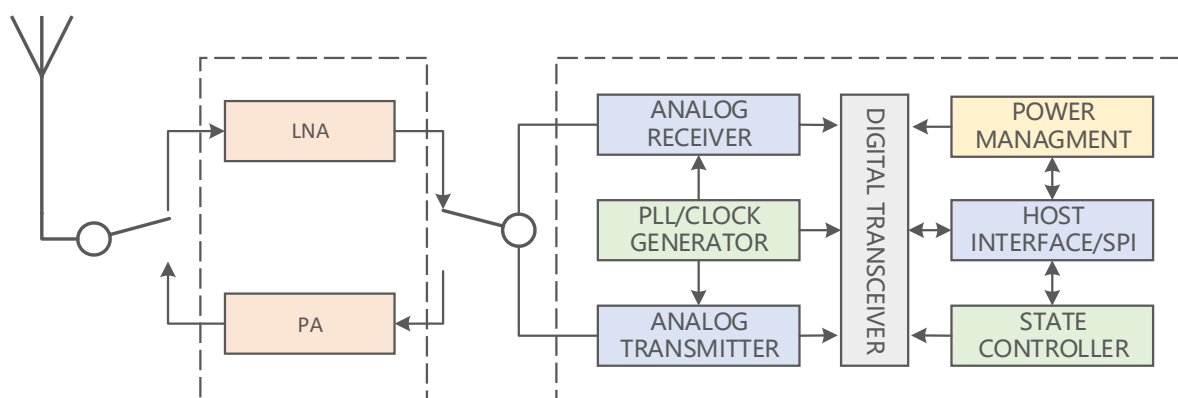
KEY FEATURES

- Comply with IEEE802.15.4-2011 ultra-wideband standard;
- Support the radio frequency band from 6.0GHz to 6.7GHz (Band 5/7);
- The output power of transmitter can be programmed and controlled; Tyically, the output power of transmitter is over-22dbm/Mhz;
- Fully coherent receiver, maximum use distance, high accuracy;
- The design complies with FCC&ETSI UWB spectrum standards;
- The power supply is 2.8V~3.6V;
- The data transmission rate is 110kbps, 850kbps, and 6.8Mbps in three modes;
- The maximum data packet length is 1023 bytes, which meets the application requirements of high data volume exchange;
- Integrated MAC support function
- Support TWR and TDOA positioning;
- The host interface is SPI;

KEY BENEFITS

- Used for object positioning in real-time positioning system with an accuracy of up to 10 cm
- **Communication and Ranging distance over 1000 meters (6.8Mbps)**
- It has a larger communication range, reducing the additional infrastructure required in RTLS (Real Time Location System);
- High multipath fading immunity;
- Enable high-density label distribution in RTLS (Real-time Location System);
- The package interface is compatible with the original DWM1000.

APPLICATIONS

- Precision real time location systems (RTLS) using TWR or TDOA schemes in a variety of markets.
- Location-aware wireless sensor networks (WSNs)

HIGH LEVEL BLOCK DIAGRAM

Content

DOCUMENT INFORMATION

Disclaimer

YCHIOT reserves the right to change product specifications without notice. As far as possible changes to functionality and specifications will be issued in product specific errata sheets or in new versions of this document. Customers are advised to log in to the official website (www.ychiot.com) for the most recent updates on this product.

LIFE SUPPORT POLICY

YCHIOT products are not authorized for use in safety−critical applications (such as life support) where a failure of the YCHIOT product would reasonably be expected to cause severe personal injury or death. YCHIOT customers using or selling YCHIOT products in such a manner do so entirely at their own risk and agree to fully indemnify YCHIOT and its representatives against any damages arising out of the use of YCHIOT products in such safety−critical applications.

Caution! ESD sensitive device. Precaution should be used when handling the device in order to prevent permanent damage.

REGULATORY APPROVALS

All products developed by the user incorporating the MAX2001 must be approved by the relevant authority governing radio emissions in any given jurisdiction prior to the marketing or sale of such products in that jurisdiction and user bears all responsibility for obtaining such approval as needed from the appropriate authorities.

1 MAX5007 OVERVIEW

The MAX5007 module is an IEEE 802.15.4-2011 UWB implementation, including Decawave DW1000 UWB transceiver, and other components reside on-module. MAX2001 enables cost effective and reduced complexity integration of UWB communications and ranging features, greatly accelerating design implementation.

1.1 MAX5007 Functional Description

The MAX5007 on board the DWM1000 is a fully integrated low-power, single chip CMOS RF transceiver IC compliant with the IEEE 802.15.4-2011 [1] UWB standard. The MAX2001 module requires no RF design as the antenna and associated analog and RF components are on the module.

The module contains an on-board 38.4 MHz reference crystal. The crystal has been trimmed in production to reduce the initial frequency error to approximately 2 ppm, using the DW1000 IC's internal on-chip crystal trimming circuit, see section 2.1.1.

Always-On (AON) memory can be used to retain MAX2001 configuration data during the lowest power operational states when the on-chip voltage regulators are disabled. This data is uploaded and downloaded automatically. Use of MAX5007 AON memory is configurable.

The on-chip voltage and temperature monitors allow the host to read the voltage on the VDDAON pin and the internal die temperature information from the MAX5007.

See the DW1000 Datasheet [2] for more detailed information on device functionality, electrical specifications and typical performance.
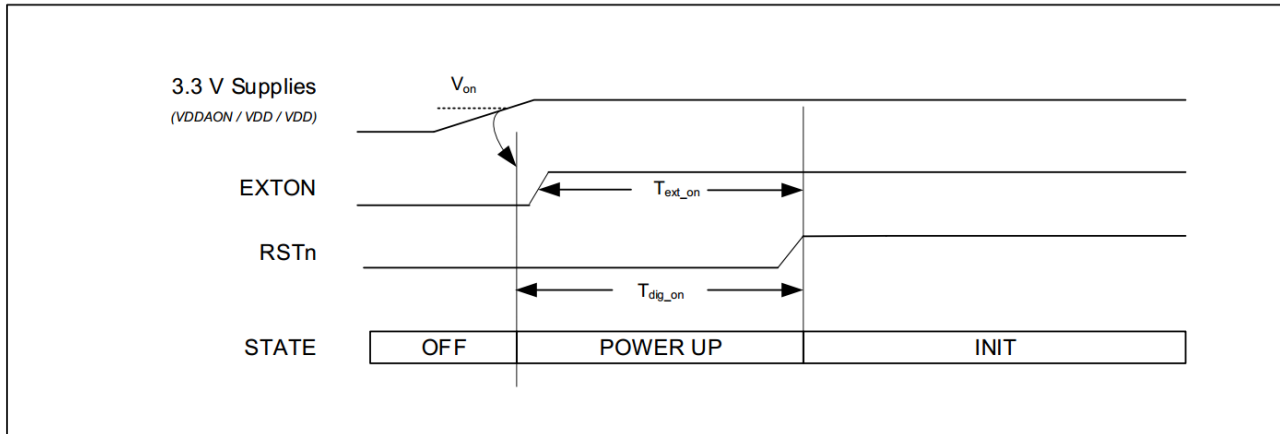
1.2 MAX5007 Power start

Figure1.2 MAX5007 Power-up Sequence

When the module starts, when the device starts to supply power, RSTn is pulled to low level by the internal integrated circuit, see the figure above . RSTn will remain low until the crystal oscillator on the module starts, and when the output of the crystal oscillator can be used by other devices on the module, RSTn turns to a high level.

Table 1: DW1000 Power-up Timings

Parameter	Description	Normal Value	Unit
V_{ON}	Voltage threshold to enable power up	2.0	V
T_{EXT_ON}	The time from when RSTn is pulled to a low level to when EXTON turns to a high level	3	ms
T_{DIG_ON}	The time required to maintain RSTn at low level through internal or external reset circuit	3	ms

RSTn may be used as an output to reset external circuitry as part of system bring-up as power is applied.

An external circuit can reset the DWM1000 by asserting RSTn for a minimum of 10 ns. RSTn is an asynchronous input. MAX2001 initialization will proceed when the pin is released to high impedance. RSTn should never be driven high by an external source. Please see DW1000 Datasheet [2] for more details of DW1000 power up.

1.3 SPI Host Interface

The DW1000 host communications interface is a slave-only SPI. Both clock polarities

(SPIPOL=0/1) and phases (SPIPHA=0/1) are supported. The data transfer protocol supports single and multiple byte read/writes accesses.All bytes are transferred MSB first and LSB last. A transfer is initiated by asserting SPICSn low and terminated when SPICSn is deasserted high.

See the DW1000 Datasheet [2] for full details of the SPI interface operation and mode configuration for clock phase and polarity.
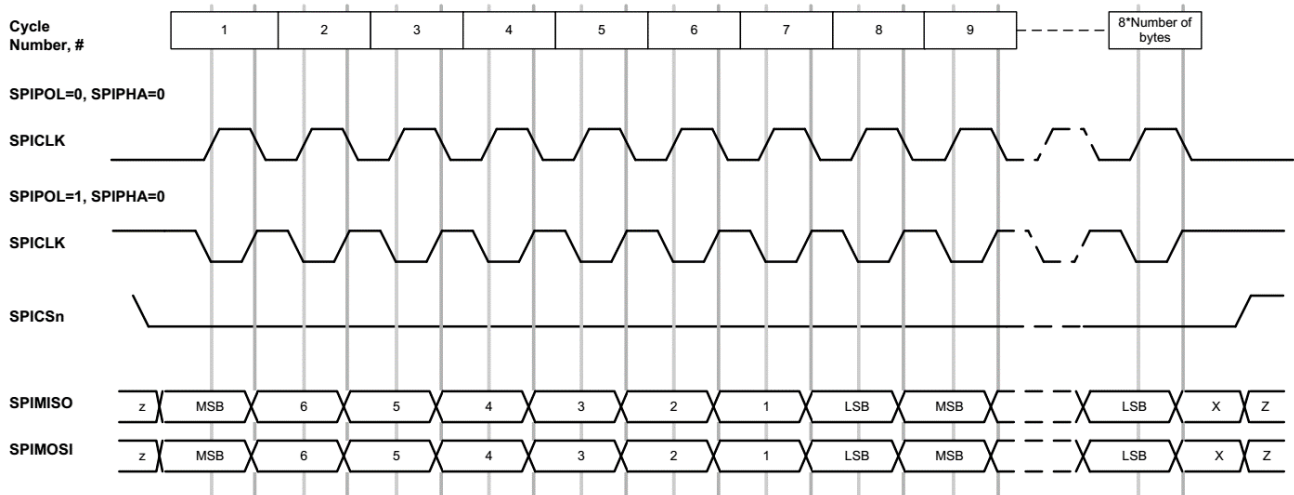
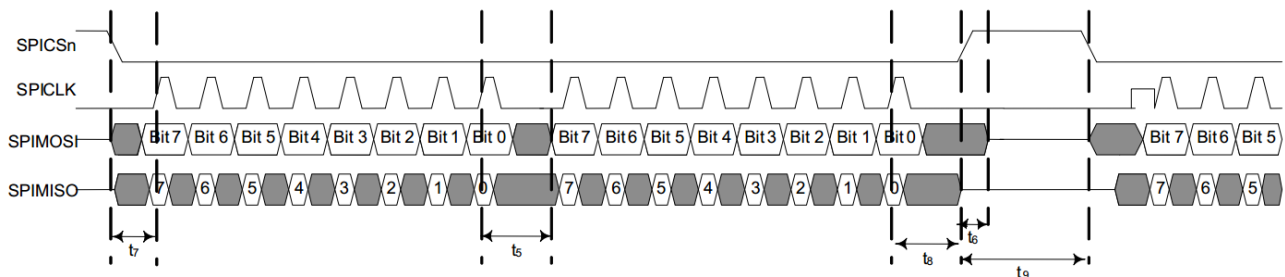Figure 1.3.1 DW1000 SPIPHA=0 Transfer Protocol
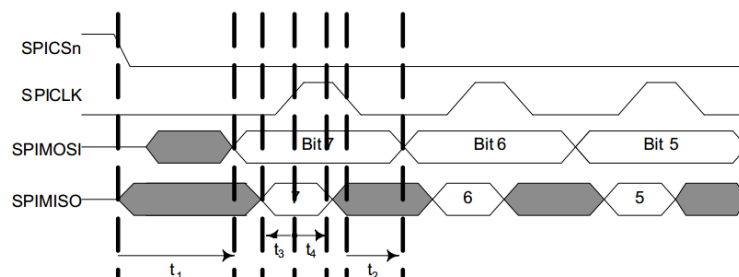
Figure 1.3.2 DW1000 SPI Timing Diagram

Figure 1.3.3 DW1000 SPI Detailed Timing Diagram

Table 1.3 MAX5007 SPI Timing Parameters

Parameter	Min.	Typ.	Max.	Unit	Description
SPICLK Period	50			ns	The maximum SPI frequency is 20 MHz when the CLKPLL is locked, otherwise the maximum SPI frequency is 3 MHz.
t_1			38	ns	SPICSn select asserted low to valid slave output data
t_2	12			ns	SPICLK low to valid slave output data
t_3	10			ns	Master data setup time
t_4	10			ns	Master data hold time
t_5	32			ns	LSB last byte to MSB next byte
t_6			10	ns	SPICSn de-asserted high to SPIMISO tri-state
t_7	16			ns	Start time; time from select asserted to first SPICLK
t_8	40			ns	Idle time between consecutive accesses
t_9	40			ns	Last SPICLK to SPICSn de-asserted

Note: TRI-State is tri-state (high level, low level, high impedance state), which refers to the three output states of the output stage

1.4 General Purpose Input Output (GPIO)

TheMAX5007 provides 8 configurable pins. On reset, all GPIO pins default to input. GPIO inputs, when appropriately configured, are capable of generating interrupts to the host processor via the IRQ signal.

GPIO0, 1, 2, & 3, as one of their optional functions, can drive LEDs to indicate the status of various chip operations. Any GPIO line being used to drive an LED in this way should be connected as shown. GPIO5 & 6 are used to configure the operating mode of the SPI as described in the DW1000 Datasheet [2]. See DW1000 Datasheet [2] and DW1000 User Manual [3] provide full details of the configuration and use of the GPIO lines.

1.5 AON Memory

Configuration retention in lowest power states is enabled in MAX5007 by provision of an Always-On (AON) memory array with a separate power supply, VDDAON. The MAX5007 may be configured to upload its configuration to AON before entering a low-power state and to download the configuration when waking up from the low – power state.

1.6 One-Time Programmable (OTP) Memory

The MAX5007 contains a 56x32 -bit user programmable OTP memory on the DW1000 device that is used to store per chip calibration information.

1.7 Interrupts and Device Status

DWM1000 has a number of interrupt events that can be configured to drive the IRQ output pin. The default IRQ pin polarity is active high. A number of status registers are provided in the system to monitor and report data of interest. See DW1000 User Manual [3] for a full description of system interrupts and their configuration and of status registers.

1.8 MAC

A number of MAC features are implemented including CRC generation, CRC checking and receive frame filtering. See the DW1000 Datasheet [2] and DW1000 User Manual [3] for full details.

2 MAX5007 CALIBRATION

2.1 MAX5007 CALIBRATION

Depending on the end-use application s and the system design,MAX5007 settings may need to be tuned. To help with this tuning a number of built in functions such as continuous wave TX and continuous packet transmission can be enabled. See the DW1000 User Manual [3] for further details.

2.1.1 MAX5007 Crystal Oscillator Trim

MAX5007 modules are calibrated at production to minimise initial frequency error to reduce carrier frequency offset between modules and thus improve receiver sensitivity. The calibration carried out at module production will trim the initial frequency offset to less than 2 ppm, typically.

2.1.2 Transmitter Calibration

In order to maximise range, MAX5007 transmit power spectral density (PSD) should be set to the maximum allowable for the geographic region in which it will be used. For most regions this is -41.3 dBm/MHz.

As the module contains an integrated antenna, the transmit power can only be measured over the air. The Effective Isotropic Radiated Power (EIRP) must be measured and the power level adjusted to ensure compliance with applicable regulations.

The MAX5007 provides the facility to adjust the transmit power in coarse and fine steps; 3 dB and 0.5 dB nominally. It also provides the ability to adjust the spectral bandwidth. These adjustments can be used to maximise transmit power whilst meeting regulatory spectral mask.

If required, transmit calibration should be carried out on a per DWM1000 module basis, see DW1000 User Manual [3] for full details.

2.1.3 Antenna Delay Calibration

In order to measure range accurately, precise calculation of timestamps is required. To do this the antenna delay must be known. The MAX5007 allows this delay to be

calibrated and provides the facility to compensate for delays introduced by PCB, external components, antenna and internal MAX5007 delays.

To calibrate the antenna delay, range is measured at a known distance using two MAX5007 systems. Antenna delay is adjusted until the known distance and reported range agree. The antenna delay can be stored in OTP memory.

Antenna delay calibration must be carried out as a once off measurement for each MAX5007 design implementation. If required, for greater accuracy, antenna delay calibration should be carried out on a per MAX5007 module basis, see DW1000 User Manual [3] for full details.

3 MAX5007 PIN CONNECTIONS

3.1 Pin Numbering

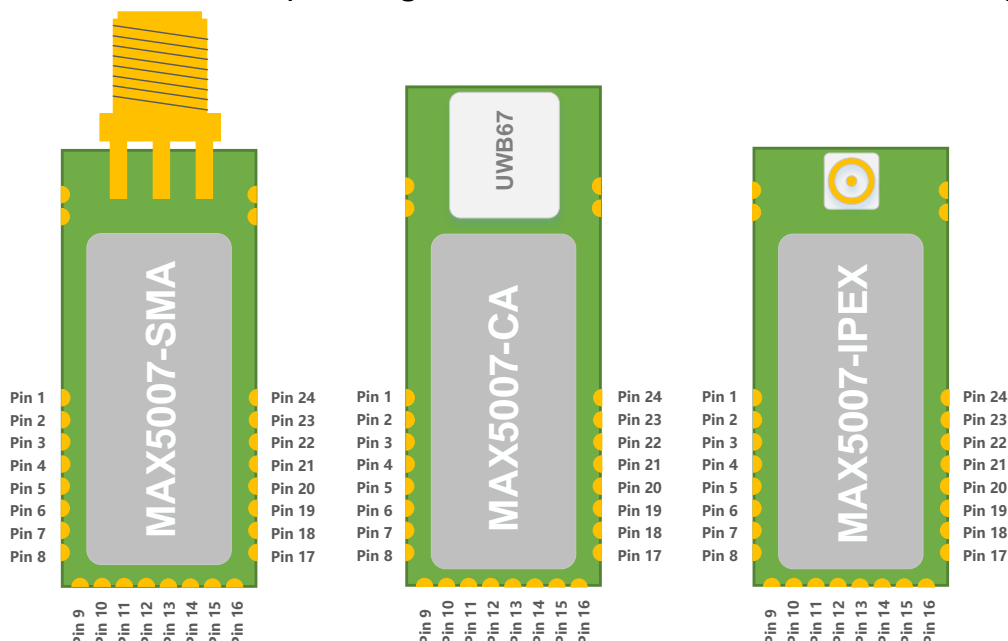MAX5007-SMA / CA / IPEX pin assignments are as follows (viewed from top):

Figure 3.1.1 MAX5007-SMA / CA / IPEX Pin Diagram\

3.2 Pin Descriptions

Table 3.2.1 MAX5007 Pin functions

SIGNAL NAME	PIN	I/O (Default)	DESCRIPTION
Digital Interface			
SPICLK	20	DI	SPI clock
SPIMISO	19	DO (O-L)	SPI data output. Refer to DW1000 Datasheet for more details [2].
SPIMOSI	18	DI	SPI data input. Refer to DW1000 Datasheet for more details [2].
SPICSn	17	DI	SPI chip select. This is an active low enable input. The high-to-low transition on SPICSn signals the start of a new SPI transaction. SPICSn can also act as a wake-up signal to bring

			DW1000 out of either SLEEP or DEEPSLEEP states Refer to DW1000 Datasheet for more details [2].
WAKEUP	2	DIO	When asserted into its active high state, the WAKEUP pin brings the DW1000 out of SLEEP or DEEPSLEEP states into operational mode. If unused, this pin can be tied to ground.
EXTON	1	DO (O-L)	External device enable. Asserted during wake up process and held active until device enters sleep mode. Can be used to control external DC-DC converters or other circuits that are not required when the device is in sleep mode so as to minimize power consumption. Refer to DW1000 Datasheet for more details [2].
IRQ / GPIO8	22	DIO (O-L)	Interrupt Request output from the DW1000 to the host processor. By default IRQ is an active-high output but may be configured to be active low if required. For correct operation in SLEEP and DEEPSLEEP modes it should be configured for active high operation. This pin will float in SLEEP and DEEPSLEEP states and may cause spurious interrupts unless pulled low. When the IRQ functionality is not being used the pin may be reconfigured as a general purpose I/O line, GPIO8.
GPIO7	4	DIO(I)	Defaults to operate as a SYNC input – refer [2]. THIS FUNCTIONALITY IS NOT APPLICABLE TO THE DW1000. This pin may be reconfigured as a general purpose I/O pin, GPIO7 under software control.
GPIO6 / SPIPHA	9	DIO(I)	General purpose I/O pin. On power-up it acts as the SPIPHA (SPI phase selection) pin for configuring the SPI mode of operation. Refer to Section 5.2.2 and the DW1000 Datasheet for more details [2]. After power-up, the pin will default to a General

			Purpose I/O pin.
GPIO5/SPIPOL	10	DIO(I)	General purpose I/O pin. On power-up it acts as the SPIPOL (SPI polarity selection) pin for configuring the SPI operation mode. Refer to Section 5.2.2 and the DW1000 Datasheet for more details [2]. After power-up, the pin will default to a General Purpose I/O pin.
GPIO4	11	DIO(I)	General purpose I/O pin.
GPIO3 / TXLED	12	DIO(I)	General purpose I/O pin. It may be configured for use as a TXLED driving pin that can be used to light a LED following a transmission. Refer to the DW1000 User Manual [2] for details of LED use.
GPIO2/RXLED	13	DIO(I)	General purpose I/O pin. It may be configured for use as a RXLED driving pin that can be used to light a LED during receive mode. Refer to the DW1000 User Manual [2] for details of LED use.
GPIO1 /SFDLED	14	DIO(I)	General purpose I/O pin. It may be configured for use as a SFDLED driving pin that can be used to light a LED when SFD (Start Frame Delimiter) is found by the receiver. Refer to the DW1000 User Manual [2] for details of LED use.
GPIO0 / RXOKLED	15	DIO(I)	General purpose I/O pin. It may be configured for use as a RXOKLED driving pin that can be used to light a LED on reception of a good frame. Refer to the DW1000 User Manual [2] for details of LED use.
RSTn	3	DIO(O-H)	Reset pin. Active Low Output. May be pulled low by external open drain driver to reset the DW1000. Refer to DW1000 Datasheet for more details [2].
Power Supplies			
VDDAON	5	P	External supply for the Always-On (AON) portion of the chip.
VDD3V3	6.7	P	3.3 V supply pins. Note that for programming the

			OTP in the DWM1000 module this voltage may be increased to a nominal value of 3.8 V for short periods.
Ground			
GND	8,16,21,23,24	G	Common ground.

Table 3.2.2 Explanation of Abbreviations

ABBREVIATION	EXPLANATION
I	Input
IO	Input / Output
O	Output
G	Ground
P	Power Supply
PD	Power Decoupling
O-L	Defaults to output, low level after reset
O-H	Defaults to output, high level after reset
I	Defaults to input.
Note: Any signal with the suffix 'n' indicates an active low signal.	

4 ELECTRICAL SPECIFICATIONS

4.1 Nominal Operating Conditions

Table 4.1 MAX5007 Operating Conditions

Parameter	Min.	Typ.	Max.	Units	Condition/Note
Operating temperature	-40		+85	℃	
Supply voltage VDDAON, VDD3V3	2.2	3.3	3.6	V	Normal operation
Supply voltage VDD3V3 for programming OTP	3.7	3.8	3.9	V	Note that for programming the OTP, the VDD3V3 voltage must be increased to 3.8 V nominal for short periods.
GPIO[0 – 7] WAKEUP RSTn SPICSn SPIMOSI SPICLK			3.6		Note that 3.6 V is the max voltage that may be applied to these pins

Note: Unit operation is guaranteed by design when operating within these ranges

4.2 DC Characteristics

Tamb = 25 ˚C, all supplies centred on typical values

Table 4.2 MAX5007 DC Characteristics

Parameter	Min.	Typ.	Max.	Units	Condition/Note
Supply current SLEEP mode		40		uA	Total current drawn from all supplies.
Supply current IDLE mode		13.4		mA	
Supply current INIT mode		3.5		mA	
TX3.3 V supplies (VDDAON, VDD)			140	mA	
RX3.3 V supplies			160	mA	Channel 5

(VDDAON, VDD)					
Digital input voltage high	0.7*VDD			V	
Digital input voltage low			0.3VDD	V	
Digital output voltage high	0.7*VDD			V	Assumes 500 Ω load
Digital output voltage low			0.3VDD	V	Assumes 500 Ω load
GPIO,IRQ, SPIMOSI ,EXTON Digital Output Drive Current	4 8 3	6 10 4		mA	

4.3 Receiver AC Characteristics

Tamb = 25 ˚C, all supplies centred on nominal values

Table 4.3 MAX5007 Receiver AC Characteristics

Parameter	Min.	Typ.	Max.	Units	Condition/Note
Frequency range	6240		6998.9	MHz	
Channel bandwidth		499		MHz	
In-band blocking level		30		dBc	Continuous wave interferer
Out-of-band blocking level		55		dBc	Continuous wave interferer

4.4 Receiver Sensitivity Characteristics

Tamb = 25 ˚C, all supplies centred on typical values. 20 byte payload. These sensitivity figures assume an antenna gain of 0 dBi and should be modified by the antenna characteristics quoted in Table 4.4 depending on the orientation of the MAX5007.

Table 4.4 MAX5007 Typical Receiver Sensitivity Characteristics

Packet Error	Data Rate	Receiver Sensitivity	Units	Condition/Note		
1%	110kbps	-102	dBm/500 MHz	Preamble 2048	Carrier frequency offset : ± 10ppm	All measurements performed on Channel
	850kpbs	-101	dBm/500 MHz	Preamble 1024		

	6.8Mbps	-93	dBm/500 MHz	Preamble 256		2,16MHz
10%	110kbps	-106	dBm/500 MHz	Preamble 2048		
	850kpbs	-102	dBm/500 MHz	Preamble 1024		
	6.8Mbps	-94	dBm/500 MHz	Preamble 256		

4.5 Reference Clock AC Characteristics

25℃，all supplies centred on typical values

Table 4.5 MAX5007 Reference Clock AC Characteristics

Parameter	Min.	Typ.	Max.	Units	Condition/Note
On-board crystal oscillator reference frequency		38.4		MHz	
On-board crystal trimming range		±25		ppm	Internally trimmed to +/- 2 ppm under typical conditions.
On-board crystal frequency stability with temperature			±30*	ppm	-40°C to +85°
On-board crystal aging			±3	ppm/3year	@25°C ±2°C
Low Power RC Oscillator	5	12	15	KHz	

*By using the temperature monitoring capability of the DW1000 chip on the MAX5007 module it is possible to dynamically trim the crystal during run time to maintain the +/- 2ppm specification over the full temperature range of operation.

4.6 Temperature and Voltage Monitor Characteristics

Table 4.6 MAX5007 Temperature and Voltage Monitor Characteristics

Parameter	Min.	Typ.	Max.	Units	Condition/Note
Voltage Monitor Range	2.4		3.75	V	
Voltage Monitor Precision		20		mV	
Voltage Monitor Accuracy		140		mV	
Temperature Monitor Range	-40		+100	℃	
Temperature Monitor Precision		0.9		℃	

4.7 Transmitter AC Characteristics

Tamb = 25 ˚C, all supplies centred on typical values

Table 4.7 Transmitter AC Characteristics

Parameter	Min.	Typ.	Max.	Units	Condition/Note
Frequency range	6240		6998.9	MHz	
Channel Bandwidths		499.2		MHz	Channel 5
Output power spectral density (programmable)		-23.0		dBm/MHz	
Power level range		37		dB	
Coarse Power level step		3		dB	
Fine Power level step		0.5		dB	
Output power variation with temperature		0.05		dB/ºC	
Output power variation with voltage		2.73		dB/V	Channel 5

Test equipment: spectrum analyzer FSL6- ROHDESCHWARZ

MAX5007 Channel 5 Transmit power spectrogram
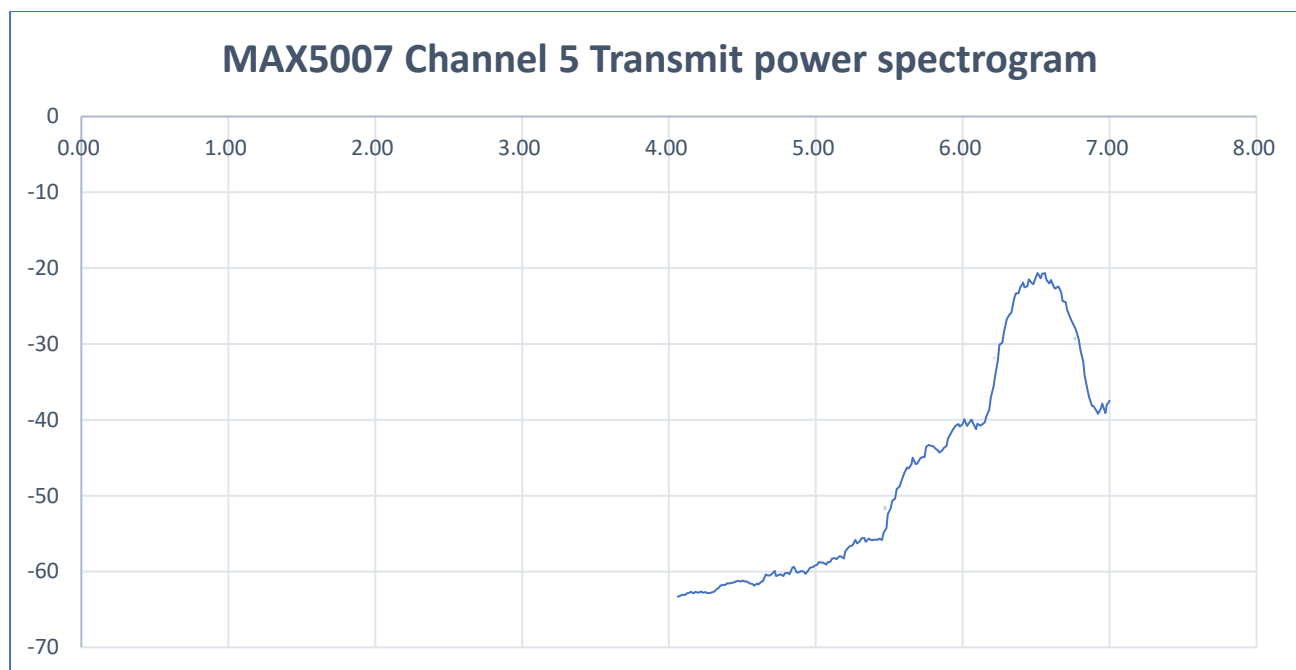
Figure 4.6.2 MAX5007-SMA Transmit power（X-axis：Ghz，Y-axis：dbm/Mhz）

4.8 Antenna Performance

MAX5007-SMA use external antenna，MAX5007-CA use built-in ceramic antenna ACS5200HFAUWB（Partron）。The parameter comparison is shown in the figure below. For more antenna selection, please refer to *ap07-YCHIOT UWB Antenna and Cable Product Specification V1.0*

Table 4.8 Comparison of external antenna and built-in ceramic antenna

Parameter	External antenna	Built-in ceramic antenna
Frequency band	3.5 ~ 8.0 GHz	3.1 ~ 8GHz
Gain	3.0dBi	2.1 ~ 2.6dBi@ (3.168GHz ~ 4.753GHz)
Input resistance	50Ω	50Ω
VSWR	≤2.2	≤2.0
Polarization mode	Vertical	Vertical
Radiation direction	Omnidirectional	Omnidirectional
Size	Total length 110mm	Length 8mm*Width 6mm*Height1mm

4.9 Absolute Maximum Ratings

Table 4.9 MAX5007 Absolute Maximum Ratings

Parameter	Min.	Max.	Units

Voltage VDD3V3 / VDDAON	-0.3	4.0	V
Receiver Power		0	dBm
Temperature - Storage temperature	-40	+85	℃
Temperature – Operating temperature	-40	+85	℃
ESD (Human Body Model)		2000	V

5 APPLICATION INFORMATION

5.1 MAX5007 Peripheral circuit design

A simple application circuit integrating MAX5007 needs to provide 3.3V power supply to VDD3V3, and the 10uF and 0.1uF decoupling capacitors should be as close as possible to the module power supply, and the SPI interface (MISO / MOSI / CS / CLK) is connected to the microcontroller, and the IRQ pin is passed 10K is pulled low, RSTn is connected to the ordinary IO port of the microcontroller, WAKEUP, EXTON and SYNC can be disconnected. Refer to Figure 5.1
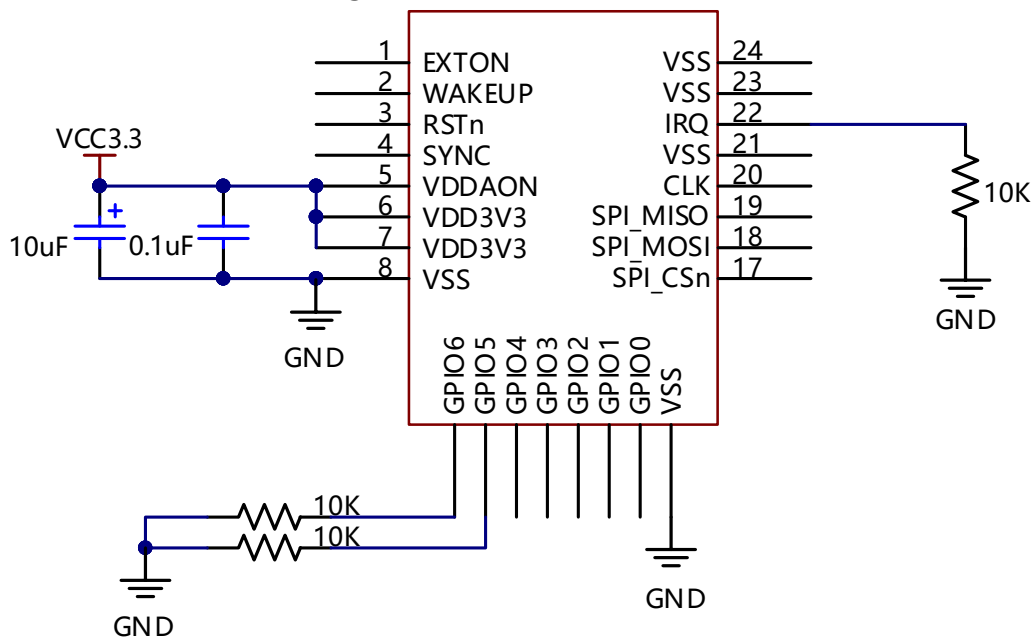
Figure 5.1 YCHIOT MAX5007 Interface and peripheral components

5.1.1 SPI Bus

The SPI signal bus and mode configuration pins may need to be treated carefully if it is desirable to connect additional SPI devices to the SPI bus, or to configure the SPI for a non-default clock polarity of phase behaviour. Please see the DW1000 Datasheet [2] for a description of all SPI clock polarity and phase configurations, referred to as SPI modes.

The SPI MISO line may be connected to multiple slave SPI devices each of which is required to go open-drain when their respective SPICSn lines are de-asserted.
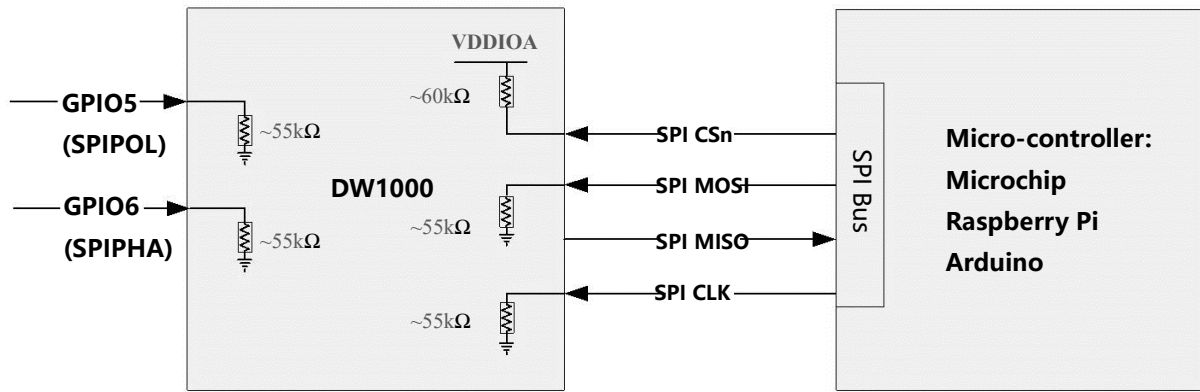
Figure 5.1.1 SPI Bus Connections

5.1.2 Configuring the SPI Mode

The SPI interface supports a number of different clock polarity and clock / data phase modes of operation. These modes are selected using GPIO5 & 6 as follows：

Table 5.1.1 DW1000 SPI Mode Configuration

GPIO 5 (SPIPOL)	GPIO 6 (SPIPHA)	SPI Mode	Description (from the master / host point of view)
0	0	0	Data is sampled on the rising (first) edge of the clock and launched on the falling (second) edge.
0	1	1	Data is sampled on the falling (second) edge of the clock and launched on the rising (first) edge.
1	0	2	Data is sampled on the falling (first) edge of the clock and launched on the rising (second) edge.
1	1	3	Data is sampled on the rising (first) edge of the clock and launched on the falling (first) edge.
Note: The 0 on the GPIO pins can either be open circuit or a pull down to ground. The 1 on the GPIO pins is a pull up to VDDIO.			

GPIO 5 / 6 are sampled / latched on the rising edge of the RSTn pin to determine the SPI mode. They are internally pulled low to configure a default SPI mode 0 without the use of external components. If a mode other than 0 is required then they should be pulled up using an external resistor of value no greater than 10 kΩ to the VDDIO output supply. MAX2001 uses GPIO5/6 to control the external PA and LNA, and requires pull-down GPIO 5/6 to connect to a 10K resistor to be pulled down to ground.

5.2   Schematic diagram of wiring between MAX5007 and MCU

Figure 5.2.1 and Figure 5.2.2 provide the connection method of MAX5007 and STM32F103T8U6/NRF52832, two single-chip microcomputers, for reference only .
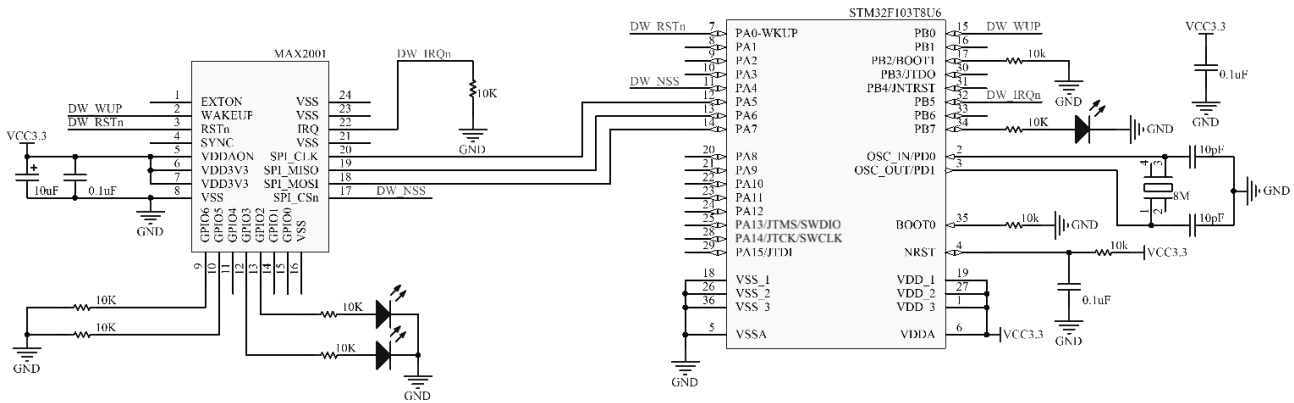
Figure 5.2.1 MAX5007 and STM32F103T8U6 wiring diagram
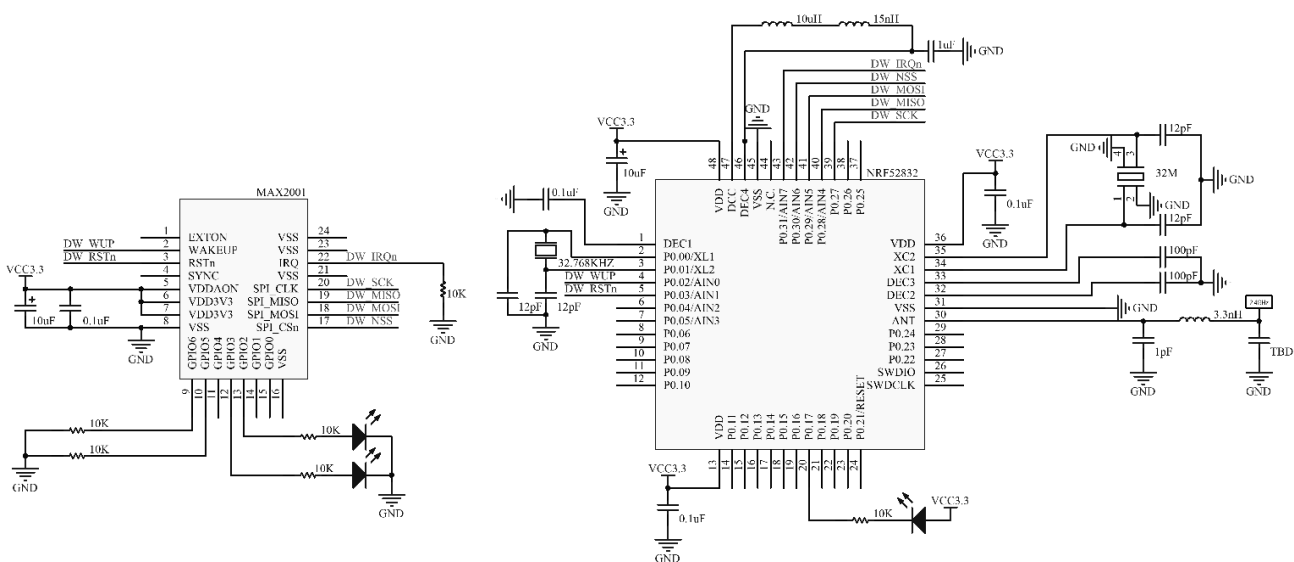
Figure 5.2.2 MAX5007 and NRF52832 wiring diagram

5.3   MAX5007 Wiring Descriptions

When designing the bottom board PCB of MAX5007, the power amplifier part and antenna part on the MAX5007 board should be kept away from metal and any materials that will affect the RF signal to clear the PCB under the module. The EMC/EMI design of the radio frequency module needs to be fully considered. YCHIOT provides the MAX5007 development evaluation kit Mini4sPlus development board, as shown in Figure 5.3.1, and provides DEMO positioning for a fee.
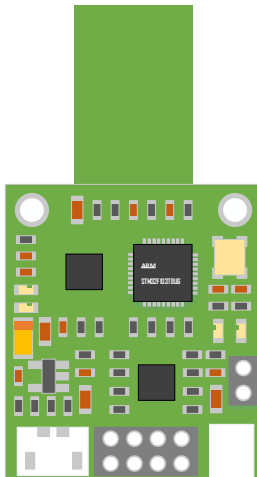
Figure 5.3.1 YCHIOT MAX5007-CA development board   Figure 5.3.2 YCHIOT MAX5007-SMA development board
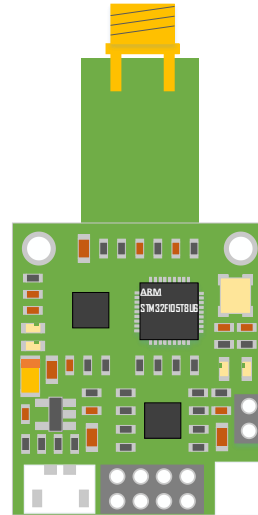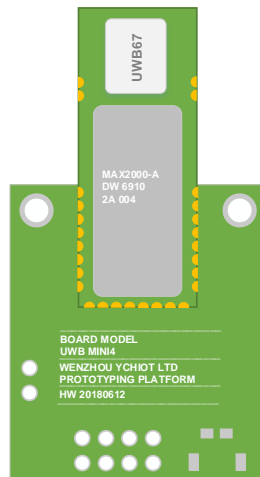
5.4 Precautions for drive control of MAX5007

5.4.1 Key control signals

Table 5.3.1 Explanation of three key control signals

Signal Name	Pin	I/O (Default)	Description
GPIO6 / EXTRXE / SPIPHA	9	DIO(I)	Genaral Ioport After power-on, it is used as the SPIPHA (SPI phase selection) pin to configure the working mode of SPI, refer to chapter 5.2.2 or DW1000 data manual. After power on, this pin can be configured as a general IO port It can also be configured as EXTRXE (External Receiver Enable) external receiver enable terminal. When configured in this mode, when DW1000 is receiving, this pin is high.
GPIO5 / EXTTXE / SPIPOL	10	DIO(I)	Genaral Ioport After power-on, it is used as the SPIPOL (SPI polarity selection) pin to configure the working mode of SPI. Refer to chapter 5.2.2 or DW1000 data manual. After power on, this pin can be

			configured as a general IO port It can also be configured as EXTTXE (External Transmit Enable) external transmit enable terminal. When configured in this mode, when DW1000 is transmitting, this pin is high.
GPIO4 / EXTPA	11	DIO(I)	Genaral Ioport It can also be configured as EXTPA (External Power Amplifier) external power amplifier enable terminal.

Note：GPIO4 / GPIO5 / GPIO6 have been configured as EXTPA, EXTTXE and EXTRXE

5.4.2 Schematic diagram of PA and LNA working principle
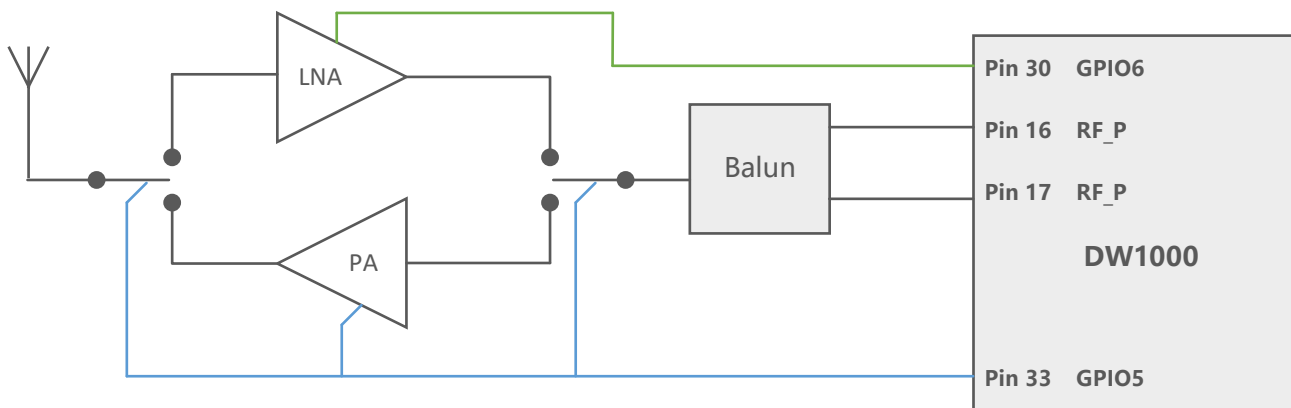
Figure 5.3 Schematic diagram of PA and LNA working principle

Table 5.3.2 GPIO5/6 Truth Table

GPIO5	GPIO 6	Mode	Status
0	0	PA close，LNA close	Idle
0	1	PA close，LNA open	Receive
1	0	PA open，LNA close	Send
1	1	Error	/

5.4.3 Code modification

Only need to turn on and off the PA and LNA at the right time to achieve the predetermined power amplifier effect. Users who use the official decaWave API functions only need make a few lines of code to changes to the program. The

following code needs to be added to the last few lines under the *dwt_initialise()* function in the *deca_device.c* file (line 253~263). For detailed register information, please refer to page 10 of the document "*aps009_dw1000_under_laes_v1.3*".

```
{
    uint32 reg;
    // Set up MFIO
    reg = dwt_read32bitreg(GPIO_CTRL_ID);
    reg |= 0x00014000 ; //7 and 8 to mode - to be used with PA
    reg |= 0x00050000 ; //8 and 9 to mode - RX/TX testing
    dwt_write32bitreg(GPIO_CTRL_ID,reg);
    //disable fine grain sequencing - this is needed when using PA on the TX
    dwt_write16bitoffsetreg(PMSC_ID,PMSC_TXFINESEQ_OFFSET,PMSC_TXFINESEQ_DIS_MASK);
}
```

5.4.4 Case Analysis

- Hardware development platform: Mini4sPlus label
- Program ranging algorithm: DS-TWR
- Test object: GPIO5 and GPIO6 of MAX5007 module
- Test instrument: ordinary oscilloscope

As shown in the figure, using our Mini4sPlus label, under the oscilloscope, T1 (yellow) represents the waveform of GPIO5, and T2 (blue) represents the waveform of GPIO6. Combining the truth table of GPIO5/6 in Table 5.3.2, it can be seen that in a TWR ranging cycle, the PA is turned on twice, respectively when the Poll command and the Final command are sent. After the tag sends the Poll, it immediately enters the receiving state, that is, GPIO6 is pulled high and the LNA is turned on.
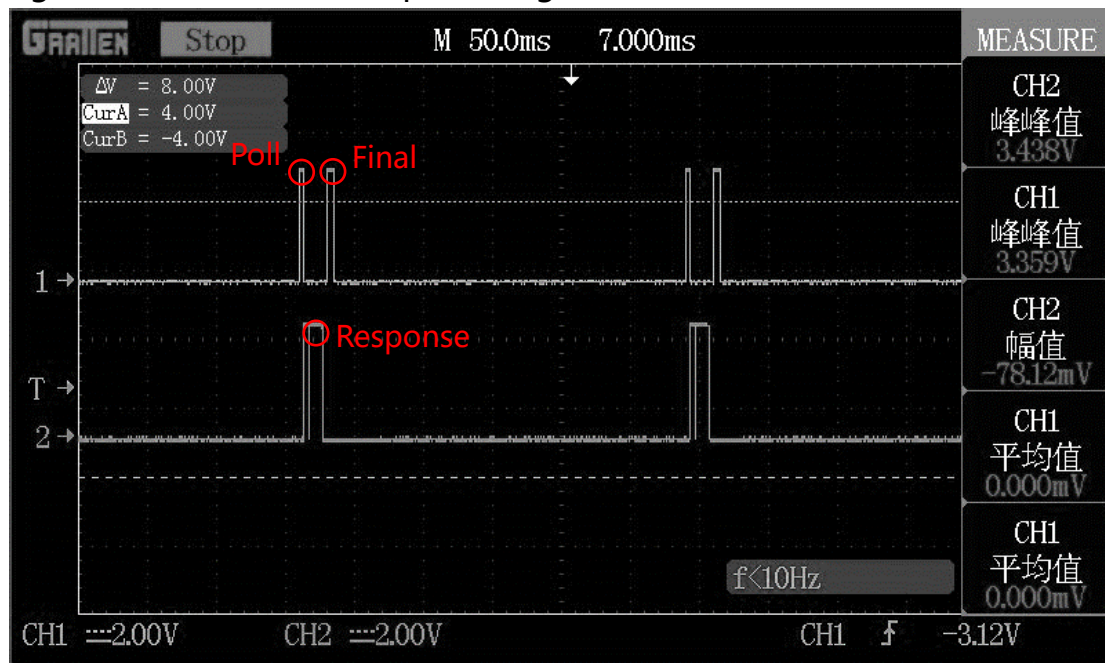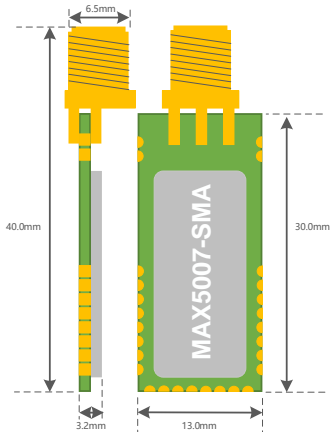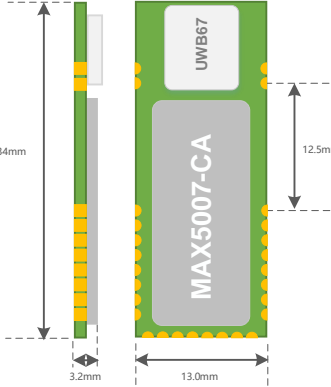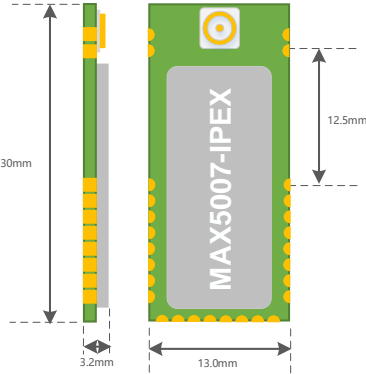

Figure 5.4 GPIO 5 and GPIO6 electrical level analysis of MAX5007 module

6 PACKAGE INFORMATION

6.1 Module Drawings

MAX5008 is a 24-pin stamp package, and the pin definition is fully compatible with DWM1000 / MAX2001. All measurements below are in millimeters.

Type	Image	Module size chart
MAX5007-SMA		
MAX5007-CA		
MAX5007-IPEX		

6.2 Recommended Module Package

Product	PCB 1	PCB 2
MAX5007 CA		
MAX5007 SMA		
MAX5007 IPEX		
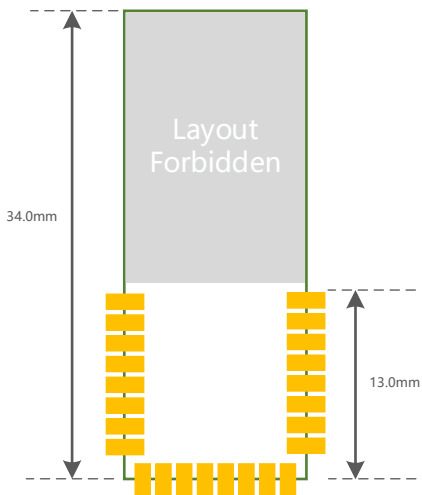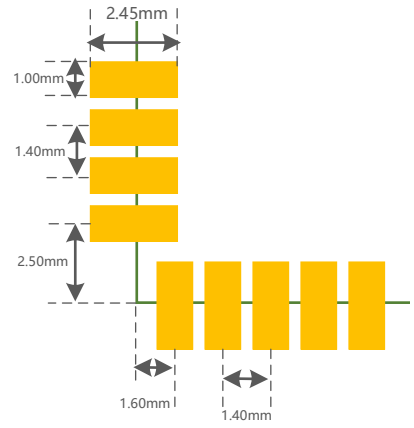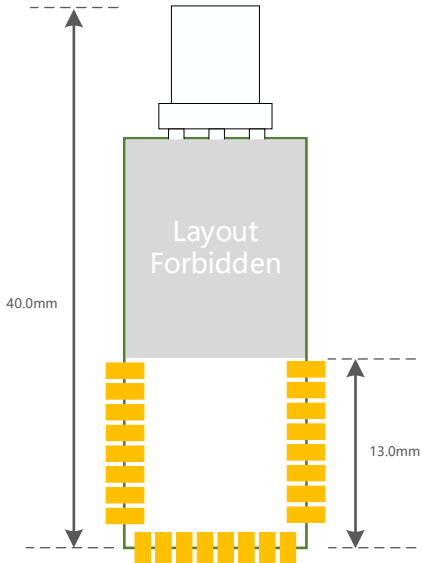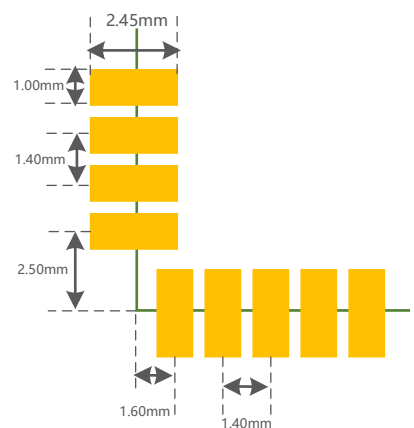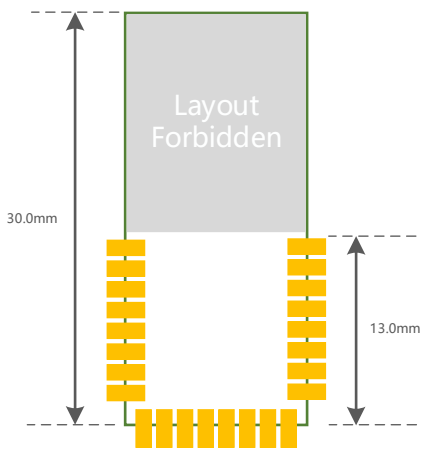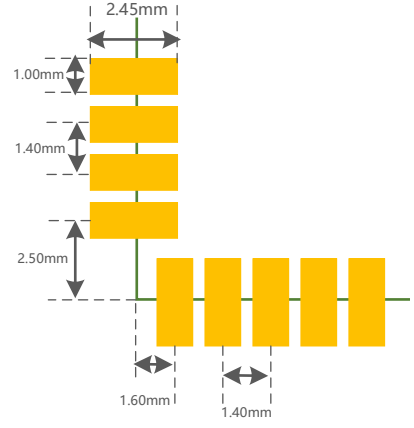
Figure 6.2 MAX5007 Land Pattern （Unit： mm）

Table 6.2 模块重量

Parameter	Min	Typical	Max	Units
Unit weight		3.2		g

6.3 Module welding curve

Manual welding is recommended for UWB module welding to avoid the internal device movement of UWB module caused by secondary reflow welding, which will affect the product performance.

If reflow soldering is necessary, it is recommended to use low-temperature solder paste for reflow soldering and add inert gas for protection. The reference temperature curve is as follows:
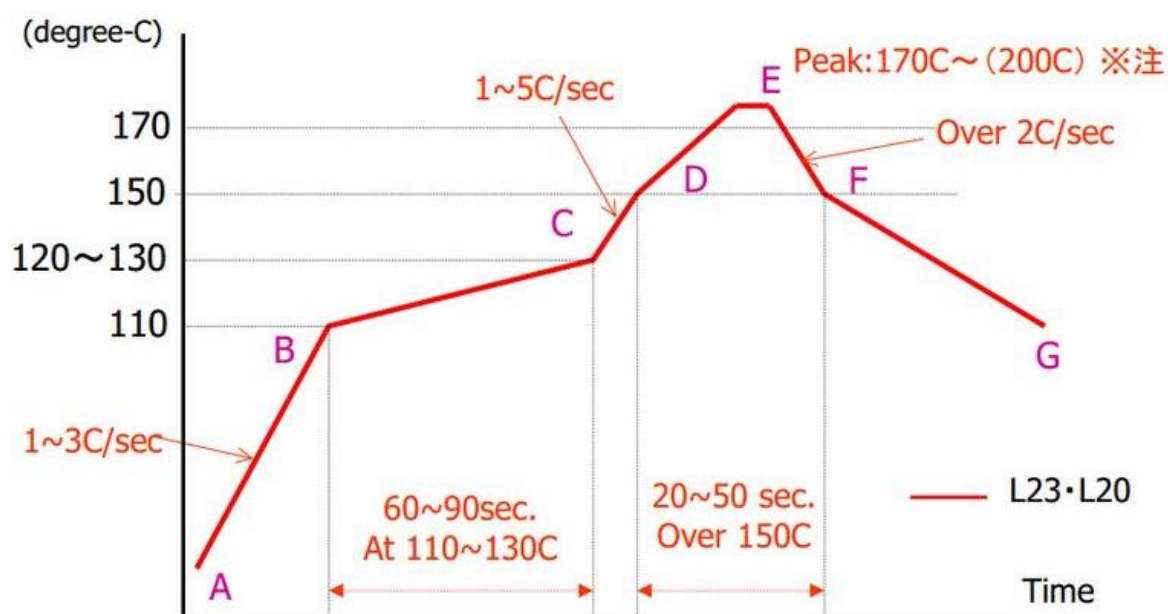

Figure 6.3 MAX5007 Module Solder Profile

融化温度

7 ORDERING INFORMATION

Product	Image	Type	Antenna interface	Status
UWB RF module		MAX5007-CA	Ceramic antenna	Will release in May 2021
UWB RF module		MAX5007-SMA	SMA Outer screw inner hole	In-stock
UWB RF module		MAX5007-IPEX	IPEX interface	Will release in May 2021

For technical question, retail and bulk purchase of MAX5007 and MAX5007 evaluation board, please contact:

- Mr.Lin 15606880772 (BD) QQ：171932915 Wechat：15606880772
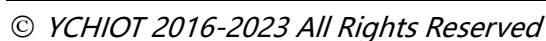- Mr.Wu 13296707815 (After sales)
- Purchase Link：https://ychiot.taobao.com/
- Official Website：http://www.ychiot.com/

8 GLOSSARY

Abbreviation	Full Title	Explanation
EIRP	Equivalent Isotropically Radiated Power	The amount of power that a theoretical isotropic antenna (which evenly distributes power in all directions) would emit to produce the peak power density observed in the direction of maximum gain of the antenna being used
ETSI	European Telecommunication Standards Institute	Regulatory body in the EU charged with the management of the radio spectrum and the setting of regulations for devices that use it
FCC	Federal Communications Commission	Regulatory body in the USA charged with the management of the radio spectrum and the setting of regulations for devices that use it
GPIO	General Purpose Input / Output	Pin of an IC that can be configured as an input or output under software control and has no specifically identified function
IEEE	Institute of Electrical and Electronic Engineers	Is the world's largest technical professional society. It is designed to serve professionals involved in all aspects of the electrical, electronic and computing fields and related areas of science and technology
LIFS	Long Inter-Frame Spacing	Defined in the context of the IEEE 802.15.4-2011 [1] standard
LNA	Low Noise Amplifier	Circuit normally found at the front-end of a radio receiver designed to amplify very low level signals while keeping any added noise to as low a level as possible
LOS	Line of Sight	Physical radio channel configuration in which there is a direct line of sight between the transmitter and the receiver

NLOS	Non Line of Sight	Physical radio channel configuration in which there is no direct line of sight between the transmitter and the receiver
PGA	Programmable Gain Amplifier	Amplifier whose gain can be set / changed via a control mechanism usually by changing register values
PLL	Phase Locked Loop	Circuit designed to generate a signal at a particular frequency whose phase is related to an incoming "reference" signal.
PPM	Parts Per Million	Used to quantify very small relative proportions. Just as 1% is one out of a hundred, 1 ppm is one part in a million
RF	Radio Frequency	Generally used to refer to signals in the range of 3 kHz to 300 GHz. In the context of a radio receiver, the term is generally used to refer to circuits in a receiver before down-conversion takes place and in a transmitter after up-conversion takes place
RTLS	Real Time Location System	System intended to provide information on the location of various items in real-time.
SFD	Start of Frame Delimiter	Defined in the context of the IEEE 802.15.4-2011 [1] standard.
SPI	Serial Peripheral Interface	An industry standard method for interfacing between IC's using a synchronous serial scheme first introduced by Motorola
TCXO	Temperature Controlled Crystal Oscillator	A crystal oscillator whose output frequency is very accurately maintained at its specified value over its specified temperature range of operation.
TWR	Two Way Ranging	Method of measuring the physical distance between two radio units by exchanging messages between the units and noting the times of transmission and reception. Refer

		to Decawave's website for further information
TDOA	Time Difference of Arrival	Method of deriving information on the location of a transmitter. The time of arrival of a transmission at two physically different locations whose clocks are synchronized is noted and the difference in the arrival times provides information on the location of the transmitter. A number of such TDOA measurements at different locations can be used to uniquely determine the position of the transmitter. Refer to Decawave's website for further information.
UWB	Ultra Wideband	UWB (Ultra Wideband) A radio scheme employing channel bandwidths of, or in excess of, 500MHz
WSN	Wireless Sensor Network	A network of wireless nodes intended to enable the monitoring and control of the physical environment

9 APPENDIX

9.1 ISO9001 Certification documents

10 DOCUMENTATION

Topic	MAX5007 LONG RANGE UWB MODULE DATASHEET
Version	V1.3
Reference	[1] IEEE802.15.4-2011 or "IEEE Std 802.15.4™-2011" (Revision of IEEE Std 802.15.4-2006). IEEE Standard for Local and metropolitan area networks - Part 15.4: Low-Rate Wireless Personal Area Networks (LRWPANs). IEEE Computer Society Sponsored by the LAN/MAN Standards Committee. Available from http://standards.ieee.org/ [2] Decawave DW1000 Datasheet www.decawave.com [3] Decawave DW1000 User Manual www.decawave.com [4] Partron(Now manufactured by Abracon) Dielectric Chip Antenna, P/N ACS5200HFAUWB (Now ACA-107-T), www.digikey.com also see www.abracon.com
Create Time	2021/04/12
Creator	Vanky Wang
Last Updated	2022/12/09

Change Person	Date	Document change record
Vanky Wang	2021-04-12	**_V1.1_** Release
Vanky Wang	2022-02-08	**_V1.2_** Update module reflow temperature curve Update ISO9001 certification documents
Lynn	2022-12-09	**_V1.3_** Update diagrams and specifications